REPLACEMENT SECTION

This listing of claims replaces all prior listings.

Listing of Claims:

1-35. (Cancelled)

36. (New) A host messaging unit for allowing asynchronous retrieval of a command from a host processor, the host messaging unit comprising:

a read controller, coupled to a bus, for determining when a host command has been provided to a host memory and for asynchronously retrieving the host command directly from a host memory via direct memory access;

a validator, coupled to the read controller, for validating the retrieved host command; and

a write controller, coupled to the bus, for asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access.

37. (New) The host messaging unit of claim 36, wherein the read controller comprises a read clock for initiating the command retrieval from the host memory at predetermined intervals.

38. (New) The host messaging unit of claim 37, wherein the read clock allows programmable predetermined intervals.

39. (New) The host messaging unit of claim 38, wherein the read clock restarts the predetermined interval after the command retrieval from the host memory.

40. (New) The host messaging unit of claim 37, wherein the write controller clears the host memory to inform the host that the host command has been read.

41. (New) The host messaging unit of claim 36, wherein the read controller comprises a busmaster command engine for initiating the command retrieval from the host memory when the busmaster command engine receives a signaled indicating host commands are available in the host memory.

42. (New) The host messaging unit of claim 41, wherein the busmaster command engine comprises a register programmable for indicating that the command is available to be retrieved from the host memory.

43. (New) A peripheral component interconnect device comprising:

a device processor; and

a host messaging unit coupled to the device processor for facilitating communication between the device processor and an external device, the host messaging unit including:

a read controller, coupled to a bus, for determining when a host command has been provided to a host memory and for asynchronously retrieving the host command directly from a host memory via direct memory access;

a validator, coupled to the read controller, for validating the retrieved host command; and

a write controller, coupled to the bus, for signaling a successful command transfer from the host memory to the host messaging unit.

44. (New) The host messaging unit of claim 43, wherein the read controller comprises a read clock for initiating the command retrieval from the host memory at predetermined intervals.

45. (New) The host messaging unit of claim 44, wherein the read clock allows programmable predetermined intervals.

46. (New) The host messaging unit of claim 45, wherein the read clock restarts the predetermined interval after the command retrieval from the host memory.

47. (New) The host messaging unit of claim 44, wherein the write controller clears the host memory to inform the host that the host command has been read.

48. (New) The host messaging unit of claim 43, wherein the read controller comprises a busmaster command engine for initiating the command retrieval from the host memory when the busmaster command engine receives a signaled indicating host commands are available in the host memory.

49. (New) The host messaging unit of claim 48, wherein the busmaster command engine comprises a register programmable for indicating that the command is available to be retrieved from the host memory.

50. (New) A method of asynchronously servicing a peripheral component interconnect device comprising:

determining when a host command has been provided to a host memory;

asynchronously retrieving the host command directly from the host memory via direct memory access;

validating the retrieved host command; and

signaling a successful command transfer from the host memory to the host messaging unit.

51. (New) The host messaging unit of claim 50, wherein the asynchronously retrieving the host command directly from the host memory via direct memory access further comprises providing a clock for initiating the retrieval of the host command from the host memory at predetermined intervals.

52. (New) The host messaging unit of claim 51, wherein the signaling a successful command transfer from the host memory to the host messaging unit further comprises clearing the host memory to inform the host that the host command has been read.

53. (New) The host messaging unit of claim 50, wherein the asynchronously retrieving the host command directly from the host memory via direct memory access further comprises initiating the command retrieval from the host memory upon receipt of a signal indicating host commands are available in the host memory.

54. (New) An article of manufacture comprising"

a program storage medium readable by a computer, the medium tangibly embodying one or more programs of instructions executable by the computer to perform operations for reducing bus transfer overhead between a host processor and a peripheral component interconnect device processor, the operations comprising:

determining when a host command has been provided to a host memory;

asynchronously retrieving the host command directly from the host memory via direct memory access;

validating the retrieved host command; and

signaling a successful command transfer from the host memory to the host messaging unit.

55. (New) A peripheral component interconnect device comprising:

a device processing means; and

a host messaging means coupled to the device processing means for facilitating communication between the device processing means and an external device, the host messaging means including:

read control means, coupled to a bus, for determining when a host command has been provided to a host memory and for asynchronously retrieving the host command directly from a host memory via direct memory access;

validating means, coupled to the read control means, for validating the retrieved host command; and

write control means, coupled to the bus, for signaling a successful command transfer from the host memory to the host messaging unit.

Authorization is hereby given to charge any required fees or credit overpayments to Deposit Account No. 50-0996 (IBMS.040US01), if necessary to complete this filing.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact attorney for Applicants, David W. Lynch, at 651-686-6633 Ext. 116.

Respectfully submitted,

Crawford Maunu PLLC
1270 Northland Drive, Suite 390
St. Paul, Minnesota 55120
651-686-6633 (x116)

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By: _____
David W. Lynch
Reg. No. 36,204